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1. **Overview of complementary GaAs technology for high-speed VLSI circuits**
Brown, R.B.; Bernhardt, B.; LaMacchia, M.; Abrokwah, J.; Parakh, P.N.; Basso, T.D.; G
Stetson, S.; Gauthier, C.R.; Foster, D.; Crawforth, B.; McQuire, T.; Sakallah, K.; Lomax
T.N.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 6, Issue 1, March 1998 Page(s):47 - 51
AbstractPlus | References | Full Text: PDF(108 KB) IEEE JNL

2. **Complementary GaAs technology for a GHz microprocessor**
Brown, R.B.; Basso, T.D.; Parakh, P.N.; Gold, S.M.; Gauthier, C.R.; Lomax, R.J.; Mudg
Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1996. Technical Digest 199
3-6 Nov. 1996 Page(s):313 - 316
AbstractPlus | Full Text: PDF(592 KB) IEEE CNF

3. **A microprocessor based power plant monitor and control system having total re capability**
Rousso, P.; Lew, P.; Gauthier, R.; Petrescu, D.; Cobo, J.; Vermette, Y.;
Telecommunications Energy Conference, 1988. INTELEC '88., 10th International
30 Oct.-2 Nov. 1988 Page(s):257 - 264
AbstractPlus | Full Text: PDF(468 KB) IEEE CNF

4. **Macro-modeling concepts for the chip electrical interface**
Amick, B.W.; Gauthier, C.R.; Liu, D.;
Design Automation Conference, 2002. Proceedings. 39th
10-14 June 2002 Page(s):391 - 394
AbstractPlus | Full Text: PDF(608 KB) IEEE CNF

5. **A 150-MOPS GaAs 8-bit slice processor**
Gauthier, R.V.; Weissman, J.; Peterson, B.E.; Florez, J.M.;
Solid-State Circuits, IEEE Journal of
Volume 23, Issue 5, Oct. 1988 Page(s):1195 - 1202
AbstractPlus | Full Text: PDF(612 KB) IEEE JNL

6. **Colif: A design representation for application-specific multiprocessor SOCs**
Cesario, W.O.; Nicolescu, G.; Gauthier, L.; Lyonnard, D.; Jerraya, A.A.;
Design & Test of Computers, IEEE
Volume 18, Issue 5, Sept.-Oct. 2001 Page(s):8 - 20

AbstractPlus | References | Full Text: PDF(160 KB) IEEE JNL

7. **A novel integrated packaging technique for high density DC-DC converters provi efficiency and thermal management**
Wanes, J.;
Applied Power Electronics Conference and Exposition, 2004. APEC '04. Nineteenth Ar Volume 2, 2004 Page(s):1229 - 1235 vol.2
AbstractPlus | Full Text: PDF(1838 KB) IEEE CNF

8. **Sixth IEEE International High-Level Design Validation and Test Workshop**
High-Level Design Validation and Test Workshop, 2001. Proceedings. Sixth IEEE Inter 7-9 Nov. 2001
AbstractPlus | Full Text: PDF(154 KB) IEEE CNF

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IEEE CNF	IEEE Conference Proceeding
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1. **A 1.3-GHz fifth-generation SPARC64 microprocessor**
Ando, H.; Yoshida, Y.; Inoue, A.; Sugiyama, I.; Asakawa, T.; Morita, K.; Muta, T.; Motol Okada, S.; Yamashita, H.; Satsukawa, Y.; Konmoto, A.; Yamashita, R.; Sugiyama, H.;
Solid-State Circuits, IEEE Journal of
Volume 38, Issue 11, Nov. 2003 Page(s):1896 - 1905
AbstractPlus | References | Full Text: PDF(1120 KB) IEEE JNL

2. **Modeling the power rails in leading edge microprocessor packages**
Michalka, T.L.;
Electronic Components and Technology Conference, 1998. 48th IEEE
25-28 May 1998 Page(s):598 - 604
AbstractPlus | Full Text: PDF(732 KB) IEEE CNF

3. **A low-cost plated column bump technology for sub 100 /spl mu/m and WLP appli**
Gupta, D.; Fria, M.; Kalle, F.;
Electronic Components and Technology, 2004. ECTC '04. Proceedings
Volume 1, 1-4 June 2004 Page(s):58 - 61 Vol.1
AbstractPlus | Full Text: PDF(512 KB) IEEE CNF

4. **Experimental method of measuring C4 die bump temperature for electronics pac**
Chau, D.S.; Chia-Pin Chiu; Torresola, J.; Prstic, S.; Reynolds, S.;
Thermal and Thermomechanical Phenomena in Electronic Systems, 2004. ITHERM '0 Intersociety Conference on
1-4 June 2004 Page(s):91 - 95 Vol.1
AbstractPlus | Full Text: PDF(527 KB) IEEE CNF

5. **Evaluation of a low-cost column bump technology for fine-pitch flip chip and WL**
Gupta, D.; Kalle, F.; Fria, M.;
Electronics Manufacturing Technology Symposium, 2004. IEEE/CPMT/SEMI 29th Inter
Jul 14-16, 2004 Page(s):18 - 21
AbstractPlus | Full Text: PDF(621 KB) IEEE CNF

6. **Design of HWSI multichip modules for quick prototyping and manufacturing**
Lee, Y.C.;
Electronic Components and Technology Conference, 1990. Proceedings., 40th
20-23 May 1990 Page(s):586 - 591 vol.1
AbstractPlus | Full Text: PDF(388 KB) IEEE CNF

7. **Design methodology for chip-on-chip applications**
Low, Y.L.; Frye, R.C.; O'Connor, K.J.;
Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging Transactions on [see also Components, Hybrids, and Manufacturing Technology, IEEE
Volume 21, Issue 3, Aug. 1998 Page(s):298 - 301
AbstractPlus | References | Full Text: PDF(172 KB) IEEE JNL

8. **A 1-GHz-clock Josephson microcomputer system**
Yano, S.; Hatano, Y.; Mori, H.; Yamada, H.; Nakahara, K.; Hirano, M.; Kawabe, U.;
Magnetics, IEEE Transactions on
Volume 27, Issue 2, Mar 1991 Page(s):2618 - 2625
AbstractPlus | Full Text: PDF(1268 KB) IEEE JNL

9. **Comparison of electroplated eutectic Bi/Sn and Pb/Sn solder bumps on various l**
Se-Young Jang; Kyung Wook Paik;
Electronics Packaging Manufacturing, IEEE Transactions on [see also Components, P
Manufacturing Technology, Part C: Manufacturing, IEEE Transactions on]
Volume 24, Issue 4, Oct. 2001 Page(s):269 - 274
AbstractPlus | References | Full Text: PDF(168 KB) IEEE JNL

10. **Modular robots**
Yim, M.; Ying Zhang; Duff, D.;
Spectrum, IEEE
Volume 39, Issue 2, Feb. 2002 Page(s):30 - 34
AbstractPlus | Full Text: PDF(537 KB) | Full Text: HTML IEEE JNL

11. **A study on coining processes of solder bumps on organic substrates**
Jae-Woong Nah; Kyung Wook Paik; Tae-Kyung Hwang; Won-Hoe Kim;
Electronics Packaging Manufacturing, IEEE Transactions on [see also Components, P
Manufacturing Technology, Part C: Manufacturing, IEEE Transactions on]
Volume 26, Issue 2, April 2003 Page(s):166 - 172
AbstractPlus | References | Full Text: PDF(1084 KB) IEEE JNL

12. **Resin flow characteristics of underfill encapsulant for flip-chip interconnection**
Yamada, H.; Togasaki, T.;
Components and Packaging Technologies, IEEE Transactions on [see also Componer
and Manufacturing Technology, Part A: Packaging Technologies, IEEE Transactions o
Volume 26, Issue 1, March 2003 Page(s):268 - 274
AbstractPlus | References | Full Text: PDF(464 KB) IEEE JNL

13. **Compact packaging of optical and electronic components for on-board optical in**
Han Seo Cho; Kun-Mo Chu; Saekyoung Kang; Sung Hwan Hwang; Byung Sup Rho; W
Joon-Sung Kim; Jang-Joo Kim; Hyo-Hoon Park;
Advanced Packaging, IEEE Transactions on [see also Components, Packaging and M
Technology, Part B: Advanced Packaging, IEEE Transactions on]
Volume 28, Issue 1, Feb 2005 Page(s):114 - 120
AbstractPlus | Full Text: PDF(872 KB) IEEE JNL

14. **Effects of substrate metallization on the degradation of flip chip interconnects u electromigration**
Wu, J.D.; Lee, C.W.; Zheng, P.J.; Li, S.;
Advanced Packaging Materials: Processes, Properties and Interfaces, 2004. Proceedir
International Symposium on
2004 Page(s):25 - 30
AbstractPlus | Full Text: PDF(4334 KB) IEEE CNF

15. **3D stacked high density packages with bumpless interconnect technology**
Lin, C.W.C.; Chiang, S.C.L.; Yang, T.K.A.;
Nuclear Science Symposium Conference Record, 2003 IEEE
Volume 1, 19-25 Oct. 2003 Page(s):73 - 77 Vol.1
AbstractPlus | Full Text: PDF(536 KB) IEEE CNF

16. **A study in flip-chip UBM/bump reliability with effects of SnPb solder compositior**
Wu, J.D.; Zheng, P.J.; Lee, C.W.; Hung, S.C.; Lee, J.J.;
Reliability Physics Symposium Proceedings, 2003. 41st Annual. 2003 IEEE Internation
30 March-4 April 2003 Page(s):132 - 139
AbstractPlus | Full Text: PDF(673 KB) IEEE CNF

17. **Processing and reliability of flip-chip on board connections**
Collier, P.A.; Teo, K.H.;
Electronic Packaging Technology Conference, 1997. Proceedings of the 1997 1st
8-10 Oct. 1997 Page(s):251 - 258
AbstractPlus | Full Text: PDF(1092 KB) IEEE CNF

18. **EMI and power delivery design in PC systems**
Herrell, D.; Beker, B.;
Electrical Performance of Electronic Packaging, 1997., IEEE 6th Topical Meeting on
27-29 Oct. 1997 Page(s):23 - 26
AbstractPlus | Full Text: PDF(332 KB) IEEE CNF

19. **A high performance SI on Si multichip module technology**
Rucker, T.G.; Mencinger, N.; Murali, V.; Regis, K.; Shukla, R.; Sundahl, R.; Siu, B.;
VLSI Technology, 1992. Digest of Technical Papers. 1992 Symposium on
2-4 June 1992 Page(s):72 - 73
AbstractPlus | Full Text: PDF(428 KB) IEEE CNF

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Michalka, T.L.;
Electronic Components and Technology Conference, 1998. 48th IEEE
25-28 May 1998 Page(s):598 - 604
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1. **Modeling of power distribution systems for high-performance microprocessors**
Herrell, D.J.; Beker, B.;
Advanced Packaging, IEEE Transactions on [see also Components, Packaging and Ma
Technology, Part B: Advanced Packaging, IEEE Transactions on]
Volume 22, Issue 3, Aug. 1999 Page(s):240 - 248
AbstractPlus | References | Full Text: PDF(236 KB) IEEE JNL

2. **Optimal retrial and timeout strategies for accessing network resources**
Libman, L.; Orda, A.;
Networking, IEEE/ACM Transactions on
Volume 10, Issue 4, Aug. 2002 Page(s):551 - 564
AbstractPlus | References | Full Text: PDF(445 KB) IEEE JNL

3. **Modeling the economics of testing: a DFT perspective**
Nag, P.K.; Gattiker, A.; Sichao Wei; Blanton, R.D.; Maly, W.;
Design & Test of Computers, IEEE
Volume 19, Issue 1, Jan.-Feb. 2002 Page(s):29 - 41
AbstractPlus | References | Full Text: PDF(180 KB) IEEE JNL

4. **Unsupervised robust nonparametric estimation of the hemodynamic response fu fMRI experiment**
Ciuciu, P.; Poline, J.-B.; Marrelec, G.; Idier, J.; Pallier, C.; Benali, H.;
Medical Imaging, IEEE Transactions on
Volume 22, Issue 10, Oct. 2003 Page(s):1235 - 1251
AbstractPlus | References | Full Text: PDF(1195 KB) IEEE JNL

5. **Tradeoffs in modeling the response of power delivery systems of high-performar microprocessors**
Beker, B.; Hirsch, T.;
Electrical Performance of Electronic Packaging, 2000, IEEE Conference on.
23-25 Oct. 2000 Page(s):77 - 80
AbstractPlus | Full Text: PDF(564 KB) IEEE CNF

6. **Model-integrated design toolset for polymorphous computer-based systems**
Eames, B.; Bapty, T.; Abbott, B.; Neema, S.; Chhokra, K.;
Engineering of Computer-Based Systems, 2003. Proceedings. 10th IEEE International Workshop on the

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1 Low power converter circuits: Feasibility of monolithic and 3D-stacked DC-DC converters for microprocessors in 90nm technology generation

Gerhard Schrom, Peter Hazucha, Jae-Hong Hahn, Volkan Kursun, Donald Gardner, Siva Narendra, Tanay Karnik, Vivek De

August 2004 **Proceedings of the 2004 international symposium on Low power electronics and design**

Full text available: pdf(225.30 KB) Additional Information: full citation, abstract, references, index terms

Rapidly increasing input current of microprocessors resulted in rising cost and motherboard real estate occupied by decoupling capacitors and power routing. We show by analysis that an on-die switching DC-DC converter is feasible for future microprocessor power delivery. The DC-DC converter can be fabricated in an existing CMOS process (90nm-180nm) with a back-end thin-film inductor module. We show that 85% efficiency and 10% output voltage droop can be achieved for 4:1, 3:1, and 2:1 conversion ...

Keywords: 3-D integration, DC-DC converter, integrated magnetics, on-die switching converter, power delivery

2 Session 10C: Embedded tutorial: IC power distribution challenges: IC power distribution challenges

Sudhakar Bobba, Tyler Thorp, Kathirgamar Aingaran, Dean Liu

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(125.96 KB) Additional Information: full citation, abstract, references, citings, index terms

With each technology generation, delivering a timevarying current with reduced nominal supply voltage variation is becoming more difficult due to increasing current and power requirements. The power delivery network design becomes much more complex and requires accurate analysis and optimizations at all levels of abstraction in order to meet the specifications. In this paper, we describe techniques for estimation of the supply voltage variations that can be used in the design of the power delive ...

3 Future performance challenges in nanometer design

Dennis Sylvester, Himanshu Kaul

June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(252.60 KB) Additional Information: full citation, abstract, references, citings, index terms

We highlight several fundamental challenges to designing high-performance integrated circuits in nanometer-scale technologies (i.e. draRita Glover, EDA Today, L.C.wn feature sizes< 100 nm). Dynamic power scaling trends lead to major packaging problems. To alleviate these concerns, tMarc Halpernhermal monitoring and feedback mechanisms can limit worst-case dissipation and reduce costs. Furthermore, a flexible multi-Vdd + multi-Vth + re-sizing approach is advocated to leverage the inherent pr ...

4 Proceedings of the SIGNUM conference on the programming environment for development of numerical software

March 1979 **ACM SIGNUM Newsletter**, Volume 14 Issue 1

Full text available: pdf(5.02 MB) Additional Information: full citation

5 Power grid design and analysis techniques: A stochastic approach To power grid analysis

Sanjay Pant, David Blaauw, Vladimir Zolotov, Savithri Sundareswaran, Rajendran Panda

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(312.28 KB) Additional Information: full citation, abstract, references, index terms

Power supply integrity analysis is critical in modern high perfor-mance designs. In this paper, we propose a stochastic approach to obtain statistical information about the collective IR and LdI/dt drop in a power supply network. The currents drawn from the power grid by the blocks in a design are modelled as stochastic processes and their statistical information is extracted, including correlation infor-mation between blocks in both space and time. We then propose a method to propagate the stat ...

Keywords: IR drop, Ldi/dt, power supply networks

6 Power distribution issues: Macro-modeling concepts for the chip electrical interface

Brian W. Amick, Claude R. Gauthier, Dean Liu

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(515.95 KB) Additional Information: full citation, abstract, references, index terms

The power delivery network is made up of passive elements in the distribution network, as well as the active transistor loads. A chip typically has three types of power supplies that require attention: core, I/O, and analog. Core circuits consist of digital circuits and have the largest current demand. In addition to all of the system issues/models for the core, modeling the I/O subsystem has the additional requirement of modeling return paths and discontinuities. The analog circuits present yet ...

Keywords: VLSI power distribution, analog and I/O power delivery, high speed microprocessor design, inductance

7 PixelFlow: the realization

John Eyles, Steven Molnar, John Poulton, Trey Greer, Anselmo Lastra, Nick England, Lee Westover

August 1997 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Full text available: pdf(1.54 MB) Additional Information: full citation, references, citings, index terms

Keywords: compositing, deferred shading, object-parallel, rendering, scalable

8 Power, buffering and open source: A fast algorithm for power grid design
Jaskirat Singh, Sachin S. Sapatnekar
April 2005 **Proceedings of the 2005 international symposium on physical design**

Full text available: pdf(232.25 KB) Additional Information: full citation, abstract, references, index terms

This paper presents an efficient heuristic algorithm to design a power distribution network of a chip by employing a successive partitioning and grid refinement scheme. In an iterative procedure, the chip area is recursively bipartitioned, and the wire pitches and the wire widths of the power grid in the partitions are repeatedly adjusted to meet the voltage drop and current density specifications. By using the macromodels of the power grid constructed in the previous levels of partitioning, the ...

Keywords: bipartitioning, locality, macromodel, optimization, power grid design, wire pitch

9 Energy and thermal-aware design: Compact thermal modeling for temperature-aware design
Wei Huang, Mircea R. Stan, Kevin Skadron, Karthik Sankaranarayanan, Shougata Ghosh, Sivakumar Velusam
June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(341.85 KB) Additional Information: full citation, abstract, references, index terms

Thermal design in sub-100nm technologies is one of the major challenges to the CAD community. In this paper, we first introduce the idea of *temperature-aware* design. We then propose a compact thermal model which can be integrated with modern CAD tools to achieve a temperature-aware design methodology. Finally, we use the compact thermal model in a case study of microprocessor design to show the importance of using temperature as a guideline for the design. Results from our thermal model s ...

Keywords: leakage, power-aware design, reliability, temperature-aware computing, temperature-aware design, thermal model

10 Power Grid and Signal Integrity Analysis: Scaling trends of on-chip Power distribution noise
Andrey V. Mezhiba, Eby G. Friedman
April 2002 **Proceedings of the 2002 international workshop on System-level interconnect prediction**

Full text available: pdf(110.79 KB) Additional Information: full citation, abstract, references, citings, index terms

The design of power distribution networks in high performance integrated circuits has become significantly more challenging with recent advances in process technology. As on-chip currents exceed tens of amperes and circuit clock periods are reduced well below a nanosecond, the signal integrity of the on-chip power supply has become a primary concern in integrated circuit design. The existing work on power distribution noise scaling is reviewed and extended to include the scaling of the inductanc ...

Keywords: power distribution, power supply noise, technology scaling

11 System-level power optimization: techniques and tools
Luca Benini, Giovanni de Micheli
April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 2

Full text available: pdf(385.22 KB) Additional Information: full citation, abstract, references, citings, index terms

This tutorial surveys design methods for energy-efficient system-level design. We consider electronic sytems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods for energy-efficient software design and compilation. This survery ...

12 On the impact of on-chip inductance on signal nets under the influence of power grid noise
T. Chen
March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(5.04 MB) Additional Information: full citation, references, index terms

13 Power grid design and analysis techniques: Optimal placement of power supply pads and pins
Min Zhao, Yuhong Fu, Vladimir Zolotov, Savithri Sundareswaran, Rajendran Panda
June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(207.21 KB) Additional Information: full citation, abstract, references, index terms

Power delivery networks of VLSI chips require adequate input supply connections to ensure reliable performance. This paper addresses the problem of finding an optimum set of pads, pins, and on-chip voltage regulators, and their placement in a given power supply network, subject to constraints on the voltage drops in the network and maximum currents through the pads, pins and regulators. The problem is modeled as a mixed integer linear program using macromodeling techniques and several heuristic ...

Keywords: pad optimization, pad placement

14 Low Power Design: Power and CAD considerations for the 1.75mbyte, 1.2ghz L2 cache on the alpha 21364 CPU
Joel Grodstein, Rachid Rayess, Tad Truex, Linda Shattuck, Sue Lowell, Dan Bailey, David Bertucci, Gabriel Bischoff, Daniel Dever, Mike Gowan, Roy Lane, Brian Lilly, Krishna Nagalla, Rahul Shah, Emily Shriver, Shi-Huang Yin, Shannon Morton
April 2002 **Proceedings of the 12th ACM Great Lakes symposium on VLSI**

Full text available: pdf(205.76 KB) Additional Information: full citation, abstract, references, index terms

A 1.75 MByte L2 cache has been designed and fabricated as part of the Alpha 21364 microprocessor[1] (Figure 1), in a .18m bulk CMOS process. The cache was designed to run at 1.2 GHz, and pass-1 samples confirm this. While Alpha CPUs are known primarily for high speed, the combination of package constraints and a tight schedule forced careful attention to the integrated whole of power expenditure and the interaction of CAD with design. The cache consumes only 7% of total die power.

Keywords: CPU, cache memory, logic verification, low-power, timing verification

15 On-chip inductance modeling

David Blaauw, Kaushik Gala, Vladimir Zolotov, Rajendran Panda, Junfeng Wang

March 2000 **Proceedings of the 10th Great Lakes symposium on VLSI**

Full text available: pdf(576.07 KB) Additional Information: full citation, abstract, references, citings, index terms

With operating frequencies approaching the gigahertz range, inductance is becoming an increasingly important consideration in the design and analysis of on-chip interconnect. We present an accurate technique for modeling and analyzing the effects of parasitic inductance on power grid noise, signal delay and crosstalk. We propose a detailed circuit model composed of interconnect resistance, inductance and distributed capacitance, device decoupling capacitances, quiescent activity in the grid, ...

16 Challenges and design choices in nanoscale CMOS

Siva G. Narendra

March 2005 **ACM Journal on Emerging Technologies in Computing Systems (JETC)**, Volume 1 Issue 1

Full text available: pdf(5.35 MB) Additional Information: full citation, abstract, references, index terms

The driving force for the semiconductor industry growth has been the elegant scaling nature of CMOS technology. In this article, we will first review the history of technology scaling that follows Moore's law from the prespective of microprocessor designs. Challenges to continue the historical scaling trends will be highlighted and design choices to address two specific challenges, process variation and leakage power, will be discussed. In nanoscale CMOS technology generations, supply and thresh ...

Keywords: CMOS, leakage power, nanoscale, process variation

17 Getting to the bottom of deep submicron II: a global wiring paradigm

Dennis Sylvester, Kurt Keutzer

April 1999 **Proceedings of the 1999 international symposium on Physical design**

Full text available: pdf(1.23 MB) Additional Information: full citation, references, citings, index terms

18 Session 10C: Embedded tutorial: IC power distribution challenges: Challenges in power-ground integrity

Shen Lin, Norman Chang

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(54.74 KB) Additional Information: full citation, abstract, references, citings, index terms

With the advance of semiconductor manufacturing, EDA, and VLSI design technologies, circuits with increasingly higher speed are being integrated at an increasingly higher density. This trend causes correspondingly larger voltage fluctuations in the on-chip power distribution network due to IR-drop, L di/dt noise, or LC resonance. Therefore, Power-Ground integrity becomes a serious challenge in designing future high-performance circuits. In this paper, we will introduce Power-Ground integrity, ad ...

19 Power grid design and analysis techniques: Efficient power/ground network analysis for power integrity-driven design methodology

Su-Wei Wu, Yao-Wen Chang

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(177.31 KB) Additional Information: full citation, abstract, references, index terms

As technology advances, the metal width is decreasing with the length increasing, making the resistance along the power line increase substantially. Together with the nonlinear scaling of the threshold voltage that makes the ratio of the threshold voltage to the supply voltage rise, the voltage (IR) drop become a serious problem in modern VLSI design. Traditional power/ground (P/G) network analysis methods are typically very computationally expensive and thus not feasible to be integrated into f ...

Keywords: footnotesize floorplanning, power/ground network

20 Highlights of ISSCC and the design of state-of-the-art microprocessors: A 1.5GHz third generation itanium® 2 processor

Jason Stinson, Stefan Rusu

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(403.60 KB) Additional Information: full citation, abstract, references, index terms

This 130nm Itanium® 2 processor implements the Explicitly Parallel Instruction Computing (EPIC) architecture and features an on-die 6MB, 24-way set associative L3 cache. The 374mm2 die contains 410M transistors and is implemented in a dual-Vt process with 6 layers copper interconnect and FSG dielectric. The processor runs at 1.5GHz at 1.3V and dissipates a maximum of 130W. This paper reviews circuit design and package details, power delivery, RAS, DFT and DFM features, as well as an overvie ...

Keywords: design methodology, on-die cache, processor, reliability, test

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